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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/837,007	04/18/2001	Mou-Shiung Lin	MEG 01-004	7677

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EXAMINER
MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 07/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/837,007	Applicant(s) LIN ET AL.4	
	Examiner James Mitchell	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/29/2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This office action is in response to the election filed May 29, 2002.

Election

2. Claims 1-12 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in Paper No. 4.

3. Applicant's election with traverse of claims 13-24 in Paper No. 4 is acknowledged. The traversal is on the ground(s) that the process claims necessarily use the product and visa versa. This is not found persuasive because the reasons for insisting on restriction as stated in MPEP 808 have been clearly met, the requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 13-16 and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamai (JP 409045691) in combination with Anonymous (RD 291011) and applicant's admitted prior art (APA).

7. Yamai (Fig 6b) discloses a semiconductor device package, comprising: a semiconductor device (1), said device having been provided with points of electrical contact (2) in an active surface thereof, said points of electrical contact having been provided with fine pitch, high reliability solder bumps (7,9), said solder bumps extending from said active surface of said semiconductor device over a height of columns of pillar metal (6), said columns of pillar metal being in contact with said points of electrical contact provided in the active surface of said semiconductor device; a BGA substrate (8) having inherent interconnect lines on said surface, said substrate having been provided with inherent points of electrical contact over a first and a second surface thereof, said points of electrical contact provided over the second surface of said substrate; said device being positioned over the second surface of said substrate, said fine pitch, high reliability solder bumps facing said second surface of said substrate (top surface of 8) providing contact between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said substrate; inherent electrical contact having been established between said fine pitch, high reliability solder bumps and said points of electrical contact provided over said second surface of said substrate; high reliability solder bumps provided to said device comprising an inherent layer of dielectric deposited over the inherent active surface of said device ("chip"), openings having been created in said layer of dielectric in a pattern overlying said points of electrical contact in an active surface of said device ("chip"), exposing the surface of said points of electrical contact in an active surface of

said device; a layer of passivation (3) deposited over the surface of said layer of dielectric, including the exposed surface of said points of electrical contact in an active surface of said device, openings having been created in said layer of passivation in a pattern overlying said points of electrical contact (2) in an active surface of said device, exposing the surface of said points of electrical contact in an active surface of said device; a layer of metal barrier (4) deposited over the surface of said layer of passivation, including the exposed surface of said points of electrical contact in an active surface of said device; pillar metal (6) and solder bumps (9) overlying said layer of barrier metal in a pattern overlying said points of electrical contact in an active surface of said device, said pillar metal and solder bumps being separated by a layer of under bump metal; and said layer of barrier metal having been etched; said barrier metal having been removed said barrier metal from the surface of said layer of passivation where said barrier layer is not covered by said pillar metal while further leaving in place said barrier layer extending from said pillar metal by a measurable amount.

8. Yamai does not show that the substrate comprises a solder mask provided over said second surface of said substrate; electrical contact provided over said second surface of said substrate by a process of solder reflow; said semiconductor device being encapsulated in a molding compound, said molding compound surrounding said device on all sides including said active surface of said device; contact balls making electrical contact with said points of electrical contact provided over said first surface of said BGA substrate electrical contact having been established between said solder balls inserted into said solder mask provided over said first surface of said BGA substrate and said

points of electrical contact provided over said first surface of said BGA substrate by a process of solder reflow.

9. However, Anonymous utilizes a solder mask ("solder dam"; F) provided over said second surface of said substrate where said mask removed from a portion of said points of electrical contact provided over the second surface of said BGA substrate by a measurable amount.

10. It would have been obvious to one of ordinary skill in the art to incorporate a solder mask over the second surface of said substrate in order to provide a dam for solder material during reflow at chip joining as taught by Anonymous (Abstract).

11. APA (Fig 1; application Page 10, 11) discloses a conventional flip chip package with a BGA substrate wherein interconnect lines provided over the second surface of said BGA substrate and said semiconductor device is encapsulated in a molding compound, said molding compound surrounding said device on all sides including said active surface of said device; contact balls making electrical contact with said points of electrical contact provided over said first surface of said BGA substrate electrical contact having been established between said solder balls inserted into said solder mask provided over said first surface of said BGA substrate and said points of electrical contact provided over said first surface of said BGA substrate.

12. It would have been obvious to one of ordinary skill in the art to incorporate with the combined package of the prior art, an encapsulant by providing a molding compound surrounding said device on all sides including said active surface of said device or to provide an underfill; and contact balls making electrical contact with said points of electrical contact provided over said first surface of said BGA substrate electrical contact having been established between said solder balls inserted into said solder mask provided over said first surface of said

BGA substrate and said points of electrical contact provided over said first surface of said BGA substrate, since conventional in flip chip type packages as admitted by applicant (Page 9 and 11).

13. With respect to claim 14, although the prior art does not appear to explicitly teach the statement of intended use of creating a channel through which cleaning solution can readily flow, the statement of intended use does not result in a structural difference between the claimed apparatus and the apparatus of the prior art. Further, because the apparatus of prior is inherently capable of being used for the intended use the statement of intended use does not patentably distinguish the claimed apparatus from the apparatus of prior art. Similarly, the manner in which an apparatus operates is not germane to the issue of patentability of the apparatus; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

14. With respect to claims 15 and 16, the prior art discloses the claimed invention except for said points of electrical contact provided in an active surface of said device comprising a peripheral pad design or center type pad design.

15. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the points of electrical contact provided in an active surface of said device comprising a peripheral pad design or center type pad design, since it has been held that

rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70 (SSPA 1950).

16. With respect to claims 19, 20 22, although the prior art does not appear to explicitly disclose the process limitations of "etching said barrier and flux removal from a gap between said second surface of said BGA substrate and said active surface of said semiconductor device having been performed after completion of flip chip assembly and solder reflow," the product of the prior art inherently possesses the structural characteristics imparted by the process limitation. See In re Fitzgerald, Sanders and Bagheri, 205 USPQ 594 (CCPA 1980).

17. With respect to claims 21 and 24, the prior art does not explicitly disclose that said points of electrical contact in an active surface of said device have a pitch of about 200 um or less or that said height of columns of pillar metal being between about 10 and 100 pm and more preferably about 50 um.

18. In any case, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725

F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

19. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamai, Anonymous and APA and further in combination with Pao et al. (U.S 5,931,371).

20. The prior art does not appear to show dummy solder bumps having been provided over the active surface of said device providing mechanical support for said device, said dummy solder bumps being provided in addition to said fine pitch, high reliability solder bumps provided to said points of electrical contact in the active surface of said device.

21. However Pao utilizes dummy solder bumps (Fig 4) with fine pitch solder balls.

22. It would have been obvious to one of ordinary skill in the art to incorporate dummy solder bumps into the modified package of the prior art in order to improve reliability as taught by Pao (Column 1, Lines 53-57).

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Mitchell whose telephone number is (703) 305-0244. The examiner can normally be reached on M-F 10:30-8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3230 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

jmm
June 29, 2002

KAMAND CUNEO
PRIMARY EXAMINER